Figure 1: Functional Block Diagram of the PCS layer in 10GBASE-R Ethernet PHY.

Data Codewords have "01" sync preamble

| 0 | 1 | 64 bit data field (scrambled) |

Mixed Data/Control frames are identified with
a "10" sync preamble. Both the coded 56-bit
payload and TYPE field are scrambled

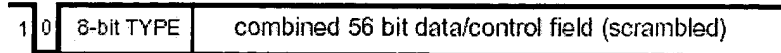| 1 | 0 | 8-bit TYPE | combined 56 bit data/control field (scrambled) |

Figure 2: 64b/66b code words.

Serial Data Input
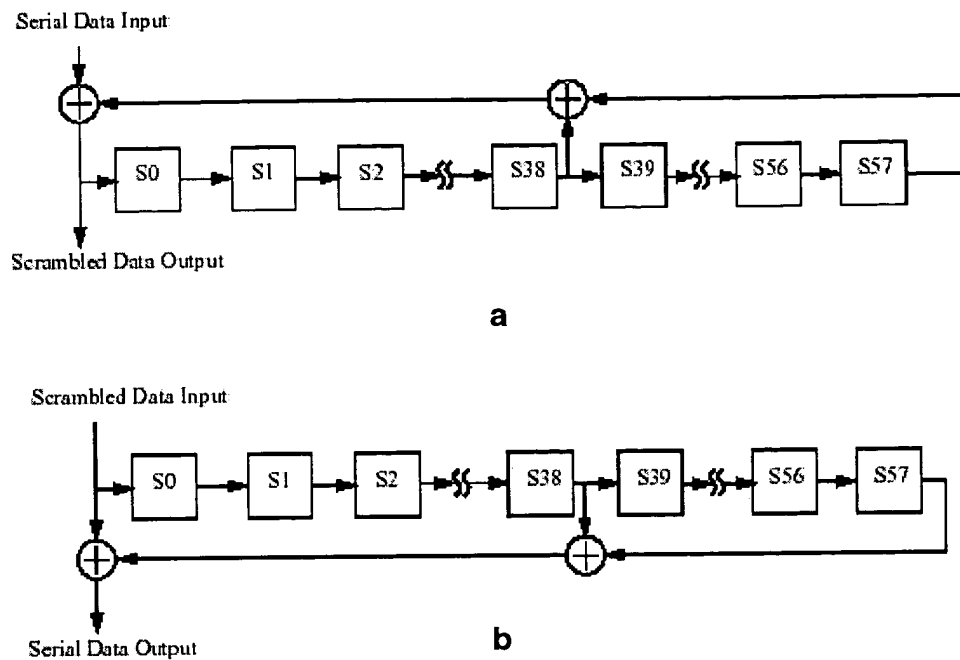
Scrambled Data Output

a

Scrambled Data Input

Serial Data Output

b

Figure 3: The self-synchronous scrambler and descrambler used in 64b/66b encoding.

Probability of packet loss with, and without error correction.
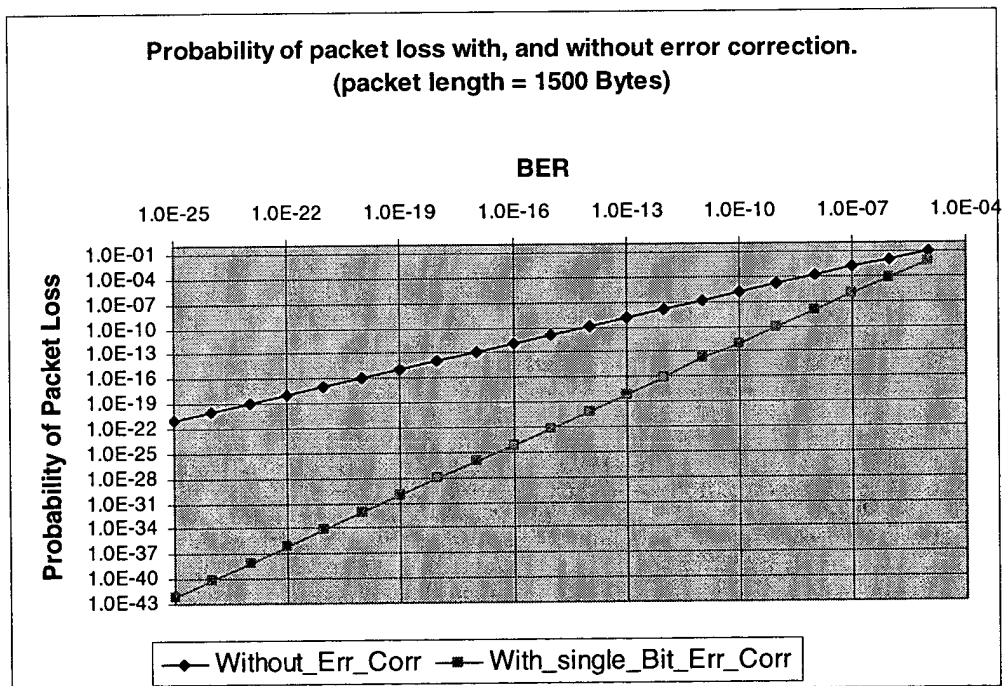(packet length = 1500 Bytes)

BER

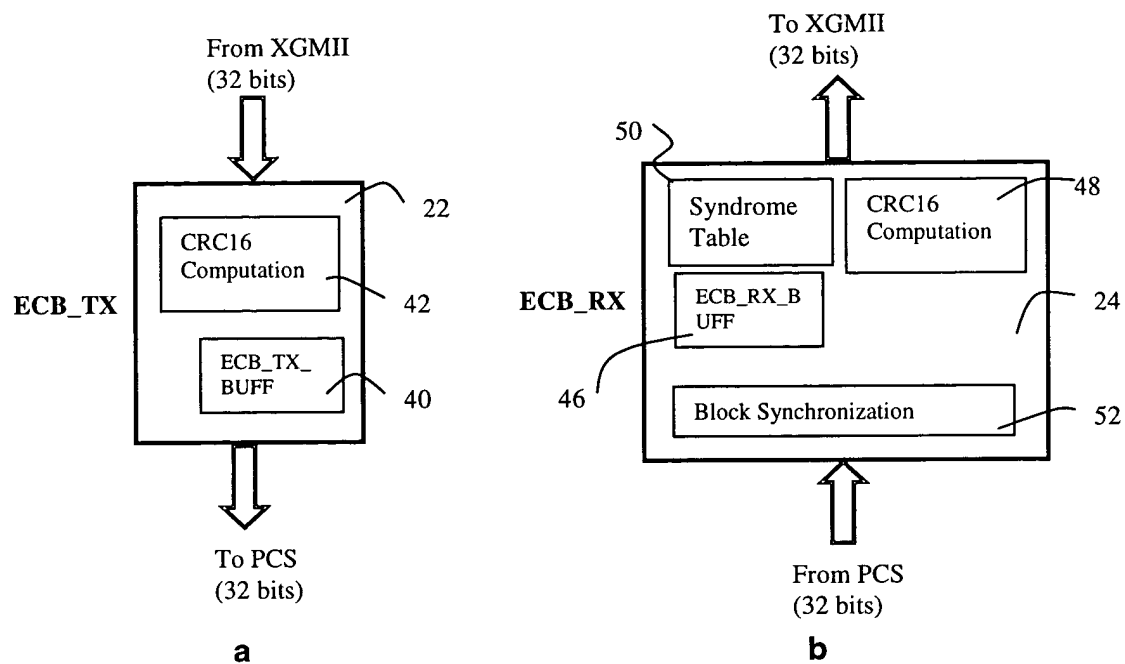**Figure 4: Probability of packet loss with, and without single-bit error correction.**

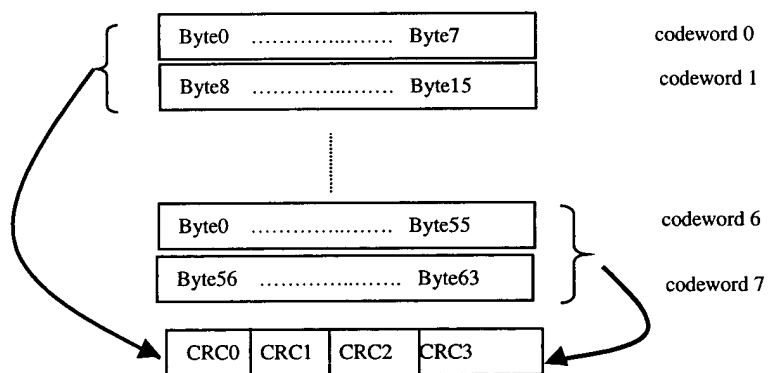**Figure 5: Functional block diagram of the Error Control Blocks (ECB).**

Figure 6: The buffer format in the ECB_RX and ECB_TX modules.
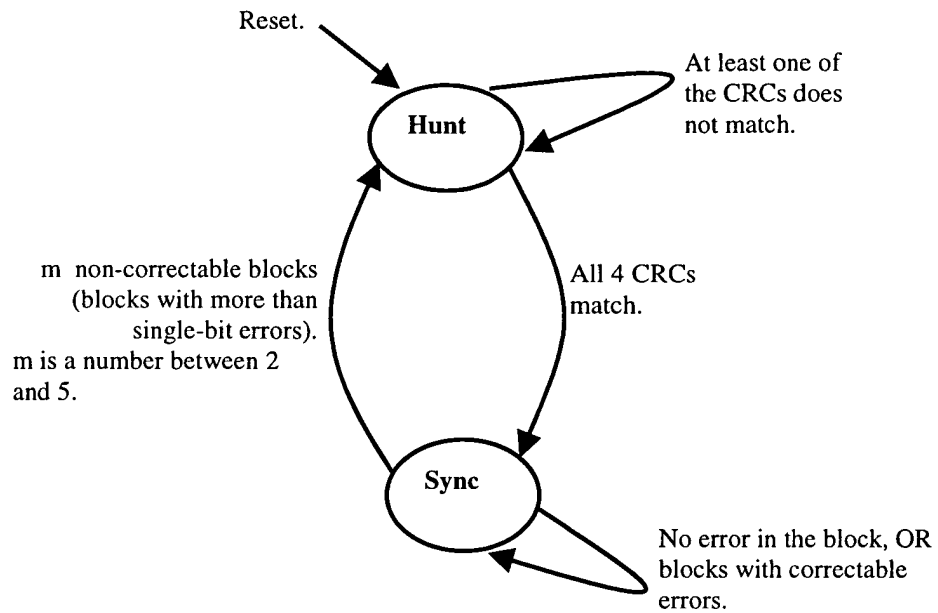
Figure 7: The state diagram of the block synchronization in the ECB_RX module.